**Module Design Document**

**For**

**ExcpnHndlg**

**04-Apr-2018**

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|  |  |  |  |
| --- | --- | --- | --- |
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| Updated the #define for ECC single bit code flash fault | Avinash James | 2.0 | 18-Apr-2016 |
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# Introduction

## Purpose

This document details the design in the FDD and also lists out any deviations which were made from the design for the implementation due to any constraints in development. ExcpnHndlg MDD describes the exception handling / reset cause determination for microcontroller diagnostics

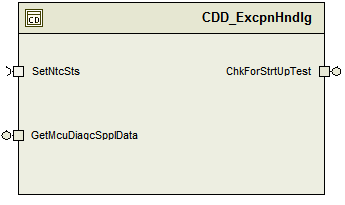
# ExcpnHndlg & High-Level Description

Refer FDD

# Design details of software module

## Graphical representation of ExcpnHndlg

## Data Flow Diagram



### Component level DFD

**N/A**

### Function level DFD

**N/A**

# Constant Data Dictionary

## Program (fixed) Constants

### Embedded Constants

#### Local Constants

|  |  |  |  |
| --- | --- | --- | --- |
| Constant Name | Resolution | Units | Value |
| FPCFGININVAL\_CNT\_T\_U32 | 1 | Counts | 0x0000001CU |
| FPCFGREGID\_CNT\_S32 | 1 | Counts | 10 |
| FPCFGSELNID\_CNT\_S32 | 1 | Counts | 0 |
| FPUINVLDOPERSTSBIT\_CNT\_U32 | 1 | Counts | ((uint32)(0x00004000U)) |
| FPUDIVBYZEROSTSBIT\_CNT\_U32 | 1 | Counts | ((uint32)(0x00002000U)) |
| FPUOVFSTSBIT\_CNT\_U32 | 1 | Counts | ((uint32)(0x00001000U)) |
| MEMERRINFOREADWRBIT\_CNT\_U32 | 1 | Counts | ((uint32)(0x00000001U)) |
| CF1STERSTRADRPARMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x00000004U)) |
| CF1STERSTRDBLBITMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x00000002U)) |
| CF1STERSTRSNGBITMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x00000001U)) |
| PRPHLBUSDATAPARMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x10000000U)) |
| DTSDBLBITMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x80000000U)) |
| CODFLSSNGBITHARDFLT\_CNT\_U08 | 1 | Counts | 1U |
| CODFLSECCDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| CODFLSADRPAR\_CNT\_U08 | 1 | Counts | 4U |
| CODFLASHEXECENAREGFAILR\_CNT\_U08 | 1 | Counts | 8U |
| MEMBISTSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 1U |
| LCLRAMECCSNGBITHARDFLT\_CNT\_U08 | 1 | Counts | 1U |
| LCLRAMECCDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| INVLDRAMAREA\_CNT\_U08 | 1 | Counts | 4U |
| DTSDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| DTSSNGBITFLT\_CNT\_U08 | 1 | Counts | 4U |
| SPI0PRPHLRAMDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| SPI1PRPHLRAMDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| SPI2PRPHLRAMDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| SPI3PRPHLRAMDBLBIT\_CNT\_U08 | 1 | Counts | 2U |
| BISTCODECCFAILR\_CNT\_U08 | 1 | Counts | 1U |
| LOGLBISTSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 4U |
| BISTNOTCMPL\_CNT\_U08 | 1 | Counts | 16U |
| CPULOCKSTEPSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 32U |
| DMALOCKSTEPSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 64U |
| FACIRSTTRFERR\_CNT\_U08 | 1 | Counts | 128U |
| LOCKSTEPCOMP\_CNT\_U08 | 1 | Counts | 1U |
| SYSVCIE\_CNT\_U08 | 1 | Counts | 2U |
| RESDOPER\_CNT\_U08 | 1 | Counts | 4U |
| ALGNREAD\_CNT\_U08 | 1 | Counts | 8U |
| ALGNWR\_CNT\_U08 | 1 | Counts | 16U |
| INSTRFETCH\_CNT\_U08 | 1 | Counts | 32U |
| INTCNCTRESDAREA\_CNT\_U08 | 1 | Counts | 64U |
| INVLDMEMACS\_CNT\_U08 | 1 | Counts | 128U |
| CLKMONR0RTLOWRLIMFLT\_CNT\_U08 | 1 | Counts | 4U |
| CLKMONR0RTUPPRLIMFLT\_CNT\_U08 | 1 | Counts | 8U |
| CLKMONR2RTLOWRLIMFLT\_CNT\_U08 | 1 | Counts | 64U |
| CLKMONR2RTUPPRLIMFLT\_CNT\_U08 | 1 | Counts | 128U |
| OPERMODERRFLSPROGMMODSTRTD\_CNT\_U08 | 1 | Counts | 1U |
| OPERMODERRTESTMODSTRTD\_CNT\_U08 | 1 | Counts | 2U |
| OPERMODERRSNGCHIPINACTV\_CNT\_U08 | 1 | Counts | 4U |
| CLKMONR1RTLOWRLIMFLT\_CNT\_U08 | 1 | Counts | 4U |
| CLKMONR1RTUPPRLIMFLT\_CNT\_U08 | 1 | Counts | 8U |
| CLKMONR3RTLOWRLIMFLT\_CNT\_U08 | 1 | Counts | 64U |
| CLKMONR3RTUPPRLIMFLT\_CNT\_U08 | 1 | Counts | 128U |
| DATAANDINSTRPROTNERR\_CNT\_U08 | 1 | Counts | 1U |
| ECMSTSFLT\_CNT\_U08 | 1 | Counts | 1U |
| EIINTRPTSTRTUPFLT\_CNT\_U08 | 1 | Counts | 2U |
| ECMMSTSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 4U |
| ECMCHKRSTRTUPTESTFAILR\_CNT\_U08 | 1 | Counts | 8U |
| ECMPSDOERRINJFLT\_CNT\_U08 | 1 | Counts | 16U |
| ECMRTMSTCHKRCOMPFLT\_CNT\_U08 | 1 | Counts | 128U |
| FPUINVLDOPEREXCPN\_CNT\_U08 | 1 | Counts | 2U |
| FPUDIVBYZEROEXCPN\_CNT\_U08 | 1 | Counts | 4U |
| FPUOVFEXCPN\_CNT\_U08 | 1 | Counts | 8U |
| FPUUKWNEXCPN\_CNT\_U08 | 1 | Counts | 16U |
| UKWNRST\_CNT\_U08 | 1 | Counts | 1U |
| UKWNECMRST\_CNT\_U08 | 1 | Counts | 2U |
| BACKUPRAMTSTFAILRINBTLDR\_CNT\_U08 | 1 | Counts | 8U |
| UKWNSWRST\_CNT\_U08 | 1 | Counts | 16U |
| BACKUPRAMTSTFAILR\_CNT\_U08 | 1 | Counts | 32U |
| FLSBTLDRPREOSSRTUPEXCPN\_CNT\_U08 | 1 | Counts | 64U |
| STRTUPRSTINFOFAILD\_CNT\_U08 | 1 | Counts | 128U |
| PROGFLOW\_CNT\_U08 | 1 | Counts | 1U |
| DEADLINEMONR\_CNT\_U08 | 1 | Counts | 2U |
| ALVMONR\_CNT\_U08 | 1 | Counts | 4U |
| WDGTOUT\_CNT\_U08 | 1 | Counts | 1U |
| PEGRTFLT\_CNT\_U08 | 1 | Counts | 2U |
| IPGRTFLT\_CNT\_U08 | 1 | Counts | 8U |
| PBGSTRTUPTSTAILR\_CNT\_U08 | 1 | Counts | 16U |
| PBGRTFLT\_CNT\_U08 | 1 | Counts | 32U |
| DBGRST\_CNT\_U08 | 1 | Counts | 1U |
| OSCRITFLT\_CNT\_U08 | 1 | Counts | 1U |
| UKWNEXCPN\_CNT\_U08 | 1 | Counts | 2U |
| OSNONCRITFLT\_CNT\_U08 | 1 | Counts | 1U |
| DMATRFERR\_CNT\_U08 | 1 | Counts | 1U |
| DMAREGACSPROTCNERR\_CNT\_U08 | 1 | Counts | 2U |
| PRPHLBUSDATAPARSTRTUPFLT\_CNT\_U08 | 1 | Counts | 64U |
| PRPHLBUSDATAPARPRTFLT\_CNT\_U08 | 1 | Counts | 128U |
| INTCVMOVERVLTGMONR\_CNT\_U08 | 1 | Counts | 1U |
| INTCVMUNDERVLTGMONR\_CNT\_U08 | 1 | Counts | 2U |
| INTMONRLOVCCFLT\_CNT\_U08 | 1 | Counts | 16U |
| EXTVLTGMONRFLT\_CNT\_U08 | 1 | Counts | 128U |
| UPPR16BITMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0xFFFF0000U)) |
| LOWR16BITMASK\_CNT\_U32 | 1 | Counts | ((uint32)(0x0000FFFFU)) |
| INTCNCTRESDAREA1UPPRADR\_CNT\_U08 | 1 | Counts | (0XFFFF4FFFU) |
| INTCNCTRESDAREA1LOWRADR\_CNT\_U08 | 1 | Counts | (0xFFFF0000U) |
| INTCNCTRESDAREA2UPPRADR\_CNT\_U08 | 1 | Counts | (0XFFFEBFFFU) |
| INTCNCTRESDAREA2LOWRADR\_CNT\_U08 | 1 | Counts | (0xFFFE0000U) |
| INTCNCTRESDAREA3UPPRADR\_CNT\_U08 | 1 | Counts | (0XFE9FFFFFU) |
| INTCNCTRESDAREA3LOWRADR\_CNT\_U08 | 1 | Counts | (0XFB000000U) |
| INTCNCTRESDAREA4UPPRADR\_CNT\_U08 | 1 | Counts | (0XF8FFFFFFU) |
| INTCNCTRESDAREA4LOWRADR\_CNT\_U08 | 1 | Counts | (0XF3000000U) |
| INVLDMEMACSUPPRADR\_CNT\_U08 | 1 | Counts | (0XFFFF7EFFU) |
| INVLDMEMACSLOWRADR\_CNT\_U08 | 1 | Counts | (0xFFFF7900U) |
| FEPCREGID\_CNT\_S32 | 1 | Counts | 2 |
| FEPCSELNID\_CNT\_S32 | 1 | Counts | 0 |
| MEAREGID\_CNT\_S32 | 1 | Counts | 6 |
| MEASELNID\_CNT\_S32 | 1 | Counts | 2 |
| NROFBRAMDATREGS\_CNT\_U08 | 1 | Counts | ((uint8)4U) |
| SIZEOFBRAMDATREGS\_CNT\_U08 | 1 | Counts | ((uint8)4U) |

# Software Component Implementation

## Sub-Module Functions

## Init: ExcpnHndlgInit1

## Design Rationale

*Non-RTE function because it needs to be called before the OS is started - so that floating point exceptions can be enabled before anything uses floating point*

## Module Outputs

*None*

## Init: ExcpnHndlgInit2

## Design Rationale

*RTE function to initialize all the NTCs to pass*

## Module Outputs

*None*

## Per: ExcpnHndlgPer1

## Design Rationale

*RTE Periodic function called every 2 ms to check for OS errors*

## Store Module Inputs to Local copies

*Refer MDD*

## (Processing of function)………

*Triggered on Timing Event every 2ms*

## Store Local copy of outputs into Module Outputs

*None*

## Server Runables

## ChkForStrtUpTest

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr0RtLowrLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr0RtUpprLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr1RtLowrLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr1RtUpprLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr2RtLowrLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr2RtUpprLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr3RtLowrLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiClkMonr3RtUpprLimFlt

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiDmaTrf

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiDmaRegAcsProtnErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiEcmMstChkrCmp

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiOperModErrFlsProgmModStrtd

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiOperModErrSngChipInactv

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiOperModErrTestModStrtd

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiPeg

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiWdg

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## FeNmiDtsEccSngBitErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## GetMcuDiagcIdnData

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## ProcMpuExcpnErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## ProcNonCritOsErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## ProcPrmntOsErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## ProcPrvlgdInstrExcpnErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## ProcUkwnExcpnErr

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## SetMcuDiagcIdnData

## Design Rationale

*Refer FDD*

## (Processing of function)………

*Refer FDD*

## Interrupt Functions

## AlgnErrIrq

## Design Rationale

*Refer FDD*

## (Processing of the ISR function)…..

*Refer FDD*

## FpuErrIrq

## Design Rationale

*Refer FDD*

## (Processing of the ISR function)…..

*Refer FDD*

## SysErrIrq

## Design Rationale

*Refer FDD*

## (Processing of the ISR function)…..

*Refer FDD*

## ResdOperIrq

## Design Rationale

*Refer FDD*

## (Processing of the ISR function)…..

*Refer FDD*

## Module Internal (Local) Functions

## ProcStrtUpOrSwRst

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | ProcStrtUpOrSwRst | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
|  |  |  |  |  |
| **Return Value** | NA |  |  |  |

## Design Rationale

*Refer FDD*

## Processing

## ProcPinRst

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | ProcPinRst | Type | Min | Max |
| **Arguments Passed** | None |  |  |  |
|  |  |  |  |  |
| **Return Value** | NA |  |  |  |

## Design Rationale

*Refer FDD*

## Processing

## McuDiagcRstChk

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | McuDiagcRstChk | Type | Min | Max |
| **Arguments Passed** | RstInfo\_Cnt\_T\_enum | McuDiagc1 | Refer FDD\* | Refer FDD\* |
|  |  |  |  |  |
| **Return Value** | McuDiagcRstChk\_Cnt\_T\_lgc | Boolean | FALSE | TRUE |

## Design Rationale

*Checks if the reset cause is power on/Flash Progamming /Hard Reset /Soft Reset.*

## Processing

Refer the FDD

## GLOBAL Function/Macro Definitions

<If these are numerous and defined in a separate source file then reference the source file only.>

## GLOBAL Function #1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function Name** | (Exact name used) | Type | Min | Max |
| **Arguments Passed** | (if none, write None) | <Refer MDD guidelines[1]> | <Refer MDD guidelines[1]> | <Refer MDD guidelines[1]> |
|  | (Insert more rows for additional passed arguments) |  |  |  |
| **Return Value** | (if no value returned, write N/A) |  |  |  |

## Design Rationale

## processing

(Place flowchart/design for local function)

# Known Limitations with Design

None

# UNIT TEST CONSIDERATION

None

Abbreviations and Acronyms

| **Abbreviation or Acronym** | **Description** |
| --- | --- |
|  |  |
|  |  |

Glossary

**Note**: Terms and definitions from the source “Nexteer Automotive” take precedence over all other definitions of the same term. Terms and definitions from the source “Nexteer Automotive” are formulated from multiple sources, including the following:

* ISO 9000
* ISO/IEC 12207
* ISO/IEC 15504
* Automotive SPICE® Process Reference Model (PRM)
* Automotive SPICE® Process Assessment Model (PAM)
* ISO/IEC 15288
* ISO 26262
* IEEE Standards
* SWEBOK
* PMBOK
* Existing Nexteer Automotive documentation

| **Term** | **Definition** | **Source** |
| --- | --- | --- |
| MDD | Module Design Document |  |
| DFD | Data Flow Diagram |  |

References

| **Ref. #** | **Title** | **Version** |
| --- | --- | --- |
| 1 | AUTOSAR Specification of Memory Mapping (Link:[AUTOSAR\_SWS\_MemoryMapping.pdf](http://www.autosar.org/download/R4.0/AUTOSAR_SWS_MemoryMapping.pdf)) | v1.3.0 R4.0 Rev 2 |
| 2 | MDD Guideline | 1.02 |
| 3 | [Software Naming Conventions.doc](http://misagweb01.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_fc55f/Software%20Naming%20Conventions%2003x(In%20Work).doc) | 1.02 |
| 4 | [Software Design and Coding Standards.doc](http://eroom1.nexteer.com/eRoomReq/Files/erooms8/NextGeneration/0_1a67a9/Software%20Design%20and%20Coding%20Standards.doc) | 2.01 |
| 5 | FDD (CM101A\_ExcpnHndlg\_Design) | See Synergy Subproject version |